Remarks

Applicant respectfully requests reconsideration of this application as amended. Claims 1, 6, and 11 have been amended. No claims have been cancelled or added. Therefore, claims 1, 4-6, 9-11, and 14-21 are presented for examination.

35 U.S.C. §102(e) Rejection

Claims 1, 4-6, 9-11, and 14-21 stand rejected under 35 U.S.C. §102(e) as being anticipated by Rozas et al. (U.S. Patent No. 6,725,361). Applicant submits that the present claims are patentable over Rozas.

Rozas discloses a floating point processor including a plurality of explicitly-addressable processor registers and an emulation register capable of storing a value used to logically rename the explicitly-addressable registers to emulate registers of a floating point stack. The processor further includes a computer-executable software process for calculating and changing a value in the emulation register to a value indicating a change in addresses of registers of the floating point stack when executing a floating point stack operation. The processor also includes adder circuitry combining a register address and the value of the emulation register in response to the computer-executable process to rename the plurality of explicitly-addressable processor registers. (Rozas at Abstract.).

Claim 1 recites:

> A method of translating instructions, said method comprising:
> translating a first block of instructions executable in a first processor architecture into a translated first block of instructions executable in a second processor architecture, said translated first block of instructions operating with a stack of data entry positions;
> during the translating, generating an expected Top of Stack (TOS) position in said stack for said first block of instructions;

during the translating, adding at least one instruction to said translated first block of instructions to determine if said first expected TOS is equal to an actual TOS position in said stack at a time of executing said translated first block of instructions; and

executing said translated first block of instructions without restarting the translating, wherein during the executing said at least one instruction to branch to correction code if said expected TOS is not equal to said actual TOS, said correction code to generate a delta of said expected TOS and said actual TOS and to adjust said stack for said first block of instructions by said delta at the time of executing said translated first block of instructions;

wherein said translated first block of instructions to continue executing after said at least one instruction adjusts said stack.

Applicant submits that Rozas does not disclose or suggest executing a translated first block of instructions without restarting a translating, wherein during the executing at least one instruction to branch to correction code if an expected TOS is not equal to an actual TOS, the correction code to generate a delta of the expected TOS and the actual TOS and to adjust a stack for the first block of instructions by the delta at the time of executing the translated first block of instructions, wherein the translated first block of instructions to continue executing after the at least one instruction adjusts the stack, as recited by claim 1.

For example, the Final Office Action relies on Rozas at column 9, lines 5-38. (Final Office Action mailed 6/30/06 at pgs. 3, point 3c-e.) This portion of Rozas provides that:

> [b]efore the succeeding translation is executed, the actual top-of-stack determined by the translation software at the completion of the preceding sequence is compared to the assumed value.... If the values differ, the operation of the processor is rolled back to the state existing at the beginning of the translation; a new translation is utilized.

(Rozas at col. 9, ll. 10-16.)

This cited portion of Rozas does not disclose the cited feature of claim 1 because it relies on a ***completely new translation to be utilized.*** The cited feature of claim 1, in comparison, adds an instruction during the translation to check for equality between expected and actual TOSs and to branch to correction code to update the expected TOS. It then proceeds to execute the translated block of instructions *without having to roll back to a previous state and utilize a new translation.* Claim 1 recites executing a translated first block of instructions *without restarting the translating.* In comparison to Rozas, the cited feature of claim 1 does not roll back to a state existing at the beginning of the translation or utilize a new translation.

Furthermore, there is no disclosure or suggestion in Rozas of an instruction in the translation ***which branches to correction code during execution of the translation in order to correct an expected TOS.*** Nor is there disclosure or suggestion of proceeding to execute the original translation after the correction. Therefore, claim 1, as well as its dependent claims, is patentable over Rozas.

Independent claims 6 and 11 also recite, in part, executing a translated first block of instructions without restarting a translating, wherein during the executing at least one instruction to branch to correction code if an expected TOS is not equal to an actual TOS, the correction code to generate a delta of the expected TOS and the actual TOS and to adjust a stack for the first block of instructions by the delta at the time of executing the translated first block of instructions, wherein the translated first block of instructions to continue executing after the at least one instruction adjusts the stack. As discussed above, Rozas does not disclose or suggest such a feature. Therefore, claims 6 and 11, as

well as their respective dependent claims, are patentable over Rozas for the reasons discussed above with respect to claim 1.

Applicant respectfully submits that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicant respectfully requests the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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Ashley R. Ott
Reg. No. 55,515

12400 Wilshire Boulevard
7th Floor
Los Angeles, California 90025-1026
(303) 740-1980